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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM62W16258B Series

4 M SRAM (256-kword × 16-bit)



ADE-203-976B (Z)
Rev. 2.0
Oct. 14, 1999

Description

The Hitachi HM62W16258B Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62W16258B Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

Features

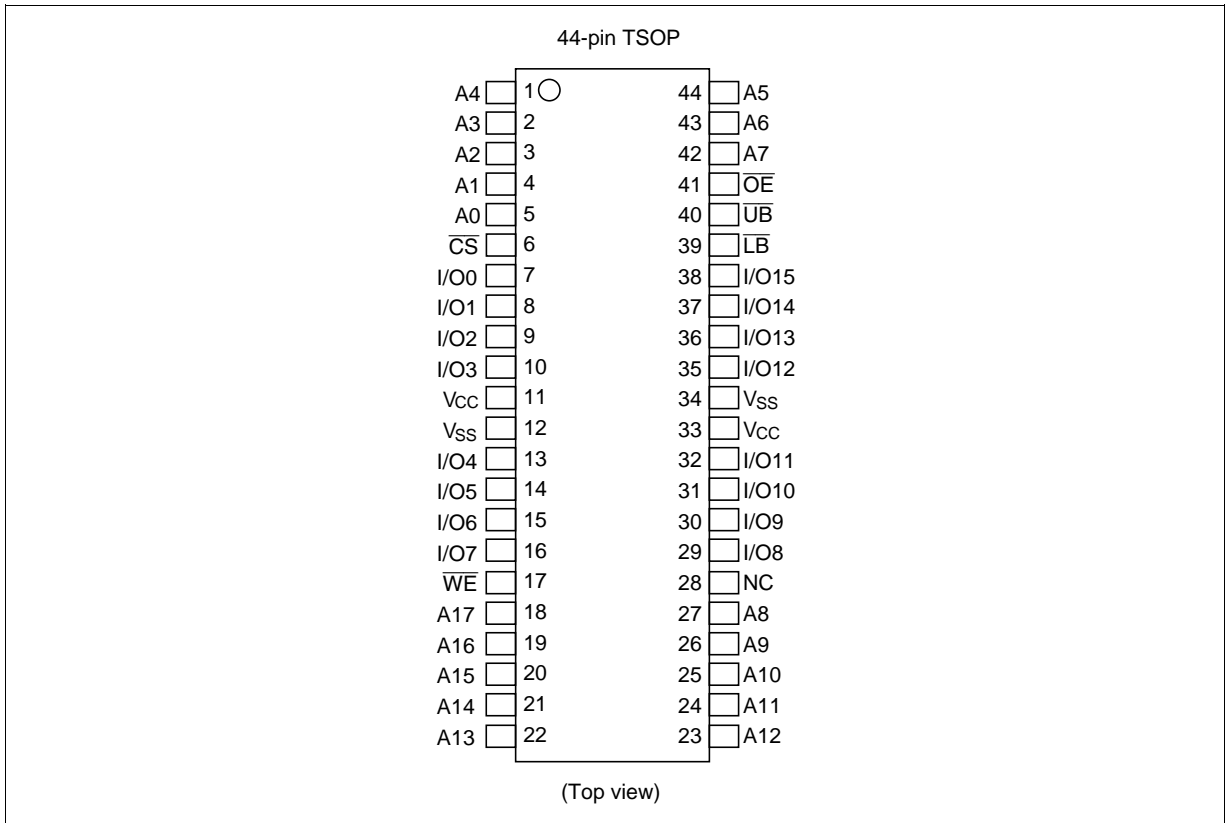
- Single 3.3 V supply: 3.3 V ± 0.3 V
- Fast access time: 55 ns/70 ns (max)
- Power dissipation:
 - Active: 9.9 mW (typ)
 - Standby: 3.3 μW (typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.

HM62W16258B Series

Ordering Information

| Type No. | Access time | Package |
|--------------------|-------------|---|
| HM62W16258BLTT-5 | 55 ns | 400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB) |
| HM62W16258BLTT-7 | 70 ns | |
| HM62W16258BLTT-5SL | 55 ns | |
| HM62W16258BLTT-7SL | 70 ns | |

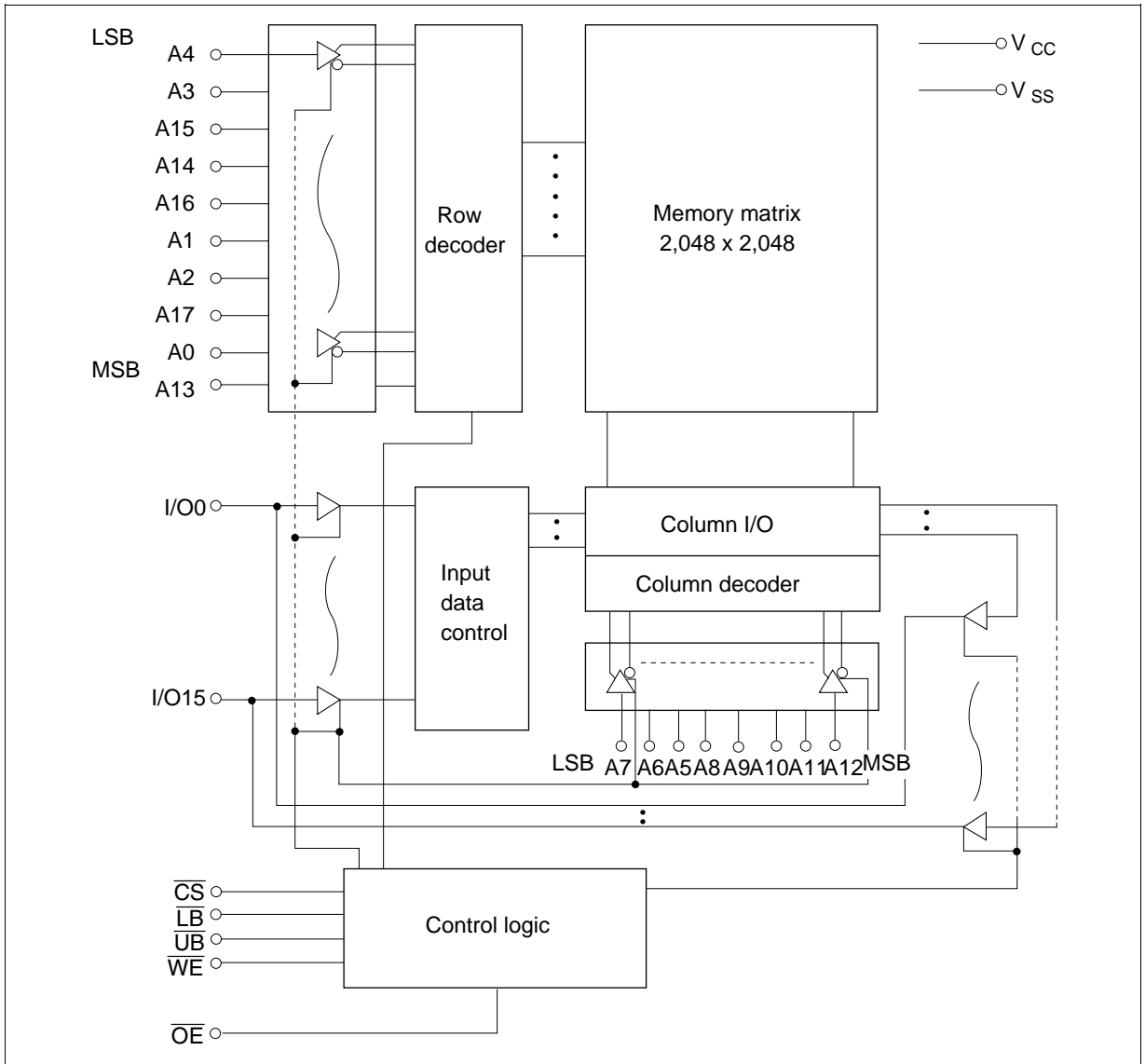
Pin Arrangement



Pin Description

| Pin name | Function |
|-----------------|-------------------|
| A0 to A17 | Address input |
| I/O0 to I/O15 | Data input/output |
| \overline{CS} | Chip select |
| \overline{WE} | Write enable |
| \overline{OE} | Output enable |
| \overline{LB} | Lower byte select |
| \overline{UB} | Upper byte select |
| V _{cc} | Power supply |
| V _{ss} | Ground |
| NC | No connection |

Block Diagram



Operation Table

| \overline{CS} | \overline{WE} | \overline{OE} | \overline{UB} | \overline{LB} | I/O0 to I/O7 | I/O8 to I/O15 | Operation |
|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|---------------|------------------|
| H | x | x | x | x | High-Z | High-Z | Standby |
| x | x | x | H | H | High-Z | High-Z | Standby |
| L | H | L | L | L | Dout | Dout | Read |
| L | H | L | H | L | Dout | High-Z | Lower byte read |
| L | H | L | L | H | High-Z | Dout | Upper byte read |
| L | L | x | L | L | Din | Din | write |
| L | L | x | H | L | Din | High-Z | Lower byte write |
| L | L | x | L | H | High-Z | Din | Upper byte write |
| L | H | H | x | x | High-Z | High-Z | Output disable |

Note: H: V_{IH} , L: V_{IL} , x: V_{IH} or V_{IL}

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|----------|---|------|
| Power supply voltage relative to V_{SS} | V_{CC} | -0.5 to +4.6 | V |
| Terminal voltage on any pin relative to V_{SS} | V_T | -0.5* ¹ to $V_{CC} + 0.3$ * ² | V |
| Power dissipation | P_T | 1.0 | W |
| Storage temperature range | Tstg | -55 to +125 | °C |
| Storage temperature range under bias | Tbias | -10 to +85 | °C |

Notes: 1. V_T min: -3.0 V for pulse half-width \leq 30 ns.
 2. Maximum voltage is +4.6 V.

DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|----------|------|-----|----------------|------|------|
| Supply voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V | |
| | V_{SS} | 0 | 0 | 0 | V | |
| Input high voltage | V_{IH} | 2.0 | — | $V_{CC} + 0.3$ | V | |
| Input low voltage | V_{IL} | -0.3 | — | 0.8 | V | 1 |
| Ambient temperature range | Ta | 0 | — | 70 | °C | |

Note: 1. V_{IL} min: -3.0 V for pulse half-width \leq 30 ns.

HM62W16258B Series

DC Characteristics

| Parameter | Symbol | Min | Typ* ¹ | Max | Unit | Test conditions | |
|---------------------------|----------------|----------------|-------------------|-----|---------------|---|--|
| Input leakage current | $ I_{LI} $ | — | — | 1 | μA | $V_{in} = V_{SS} \text{ to } V_{CC}$ | |
| Output leakage current | $ I_{LO} $ | — | — | 1 | μA | $\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH} \text{ or } \overline{WE} = V_{IL} \text{, or } \overline{LB} = \overline{UB} = V_{IH}, V_{I/O} = V_{SS} \text{ to } V_{CC}$ | |
| Operating current | I_{CC} | — | — | 20 | mA | $\overline{CS} = V_{IL}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0 \text{ mA}$ | |
| Average operating current | HM62W16258B-5 | I_{CC1} | — | — | 80 | mA | Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}$, $\overline{CS} = V_{IL}$, Others = V_{IH}/V_{IL} |
| | HM62W16258B-7 | I_{CC1} | — | — | 70 | mA | |
| | | I_{CC2} | — | 3 | 15 | mA | Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0 \text{ mA}$, $\overline{CS} \leq 0.2 \text{ V}$, $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $V_{IL} \leq 0.2 \text{ V}$ |
| Standby current | I_{SB} | — | — | 0.3 | mA | $\overline{CS} = V_{IH}$ | |
| Standby current | I_{SB1}^{*2} | — | 1 | 40 | μA | $0 \text{ V} \leq V_{in}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ | |
| | I_{SB1}^{*3} | — | 1 | 20 | μA | | |
| Output high voltage | V_{OH} | 2.4 | — | — | V | $I_{OH} = -1 \text{ mA}$ | |
| | | $V_{CC} - 0.2$ | — | — | V | $I_{OH} = -100 \mu\text{A}$ | |
| Output low voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 2 \text{ mA}$ | |
| | | — | — | 0.2 | V | $I_{OL} = 100 \mu\text{A}$ | |

Notes: 1. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | Note |
|--------------------------|-----------|-----|-----|-----|-------------|-------------------------|------|
| Input capacitance | C_{in} | — | — | 8 | pF | $V_{in} = 0 \text{ V}$ | 1 |
| Input/output capacitance | $C_{I/O}$ | — | — | 10 | pF | $V_{I/O} = 0 \text{ V}$ | 1 |

Note: 1. This parameter is sampled and not 100% tested.

Write Cycle

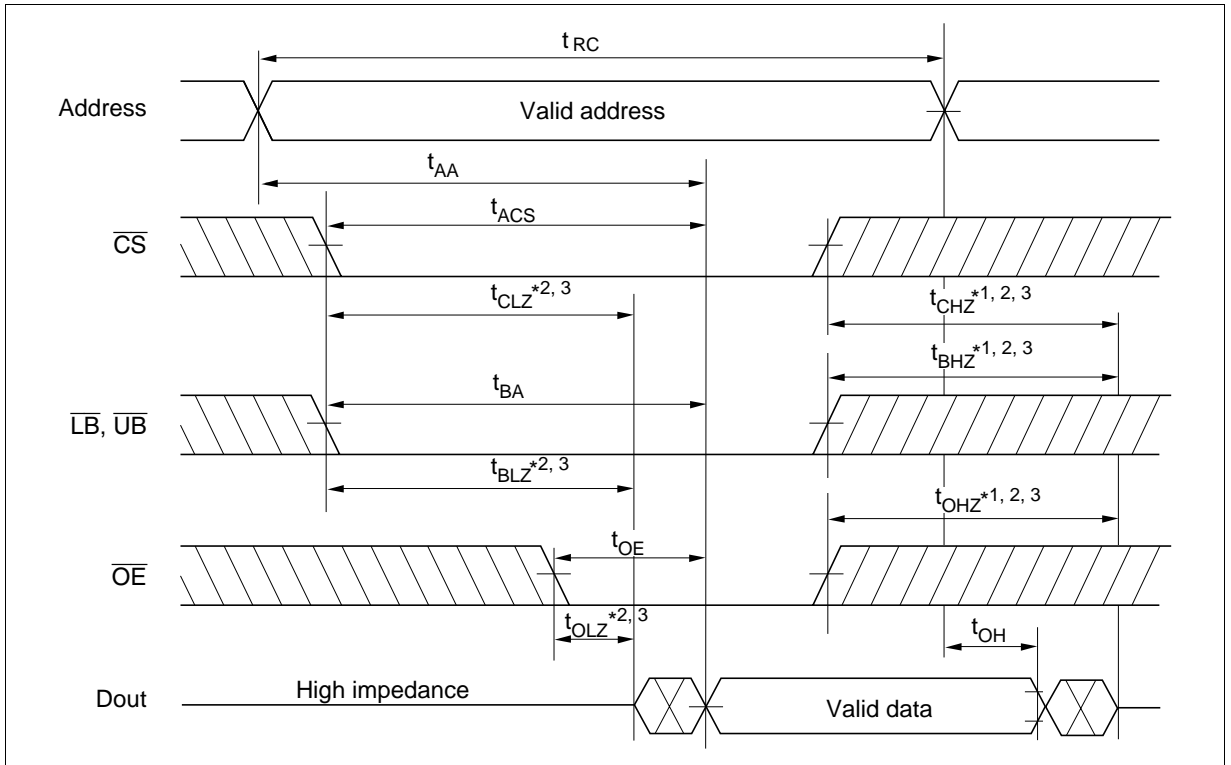
HM62W16258B

| Parameter | Symbol | -5 | | -7 | | Unit | Notes |
|---|-----------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Write cycle time | t_{WC} | 55 | — | 70 | — | ns | |
| Address valid to end of write | t_{AW} | 50 | — | 60 | — | ns | |
| Chip selection to end of write | t_{CW} | 50 | — | 60 | — | ns | 5 |
| Write pulse width | t_{WP} | 40 | — | 50 | — | ns | 4 |
| \overline{LB} , \overline{UB} valid to end of write | t_{BW} | 50 | — | 55 | — | ns | |
| Address setup time | t_{AS} | 0 | — | 0 | — | ns | 6 |
| Write recovery time | t_{WR} | 0 | — | 0 | — | ns | 7 |
| Data to write time overlap | t_{DW} | 25 | — | 30 | — | ns | |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | ns | |
| Output active from end of write | t_{OW} | 5 | — | 5 | — | ns | 2 |
| Output disable to output in High-Z | t_{OHZ} | 0 | 20 | 0 | 25 | ns | 1, 2 |
| Write to output in high-Z | t_{WHZ} | 0 | 20 | 0 | 25 | ns | 1, 2 |

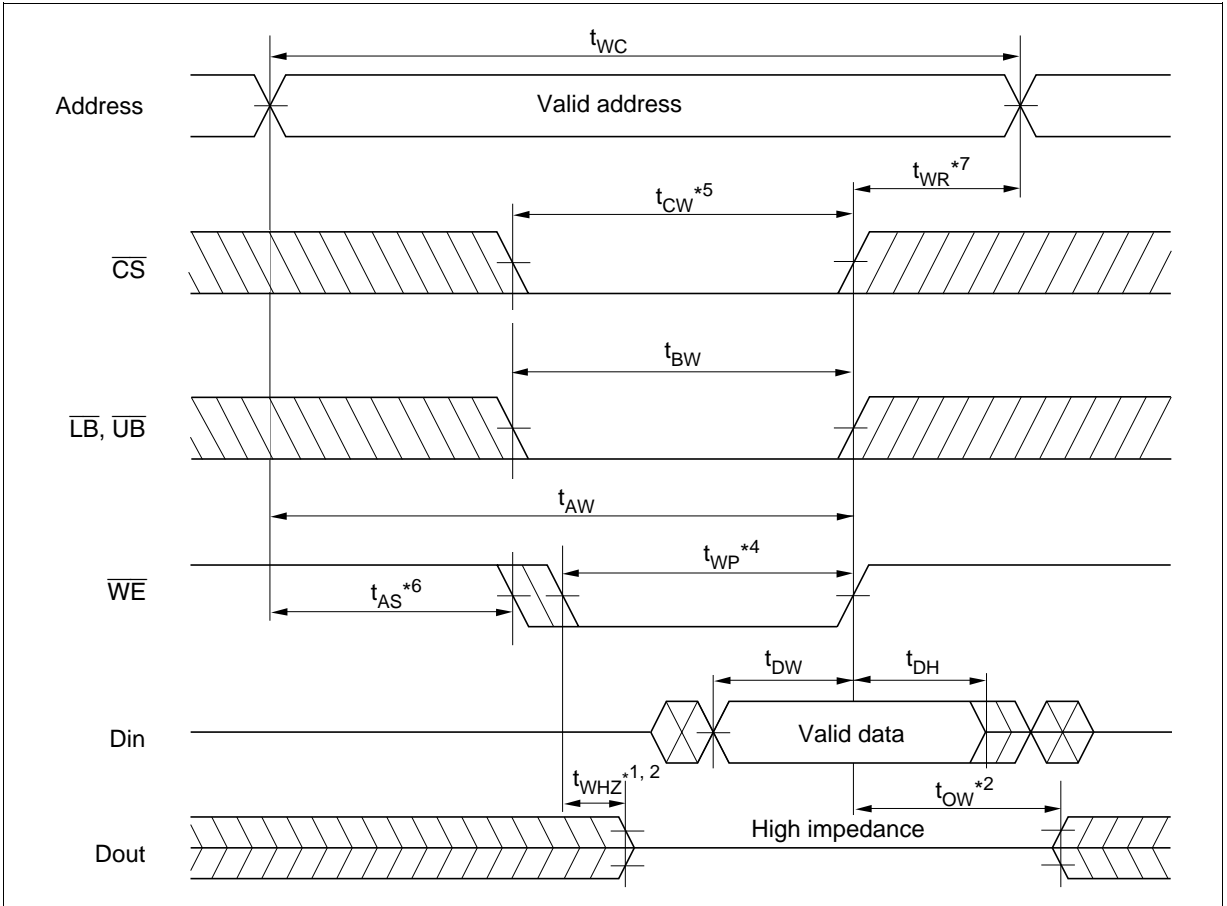
- Notes:
- t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 - A write occurs during the overlap of a low \overline{CS} , a low \overline{WE} and a low \overline{LB} or a low \overline{UB} . A write begins at the latest transition among \overline{CS} going low, \overline{WE} going low and \overline{LB} going low or \overline{UB} going low. A write ends at the earliest transition among \overline{CS} going high, \overline{WE} going high and \overline{LB} going high or \overline{UB} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from the later of \overline{CS} going low to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earliest of \overline{CS} or \overline{WE} going high to the end of write cycle.

Timing Waveform

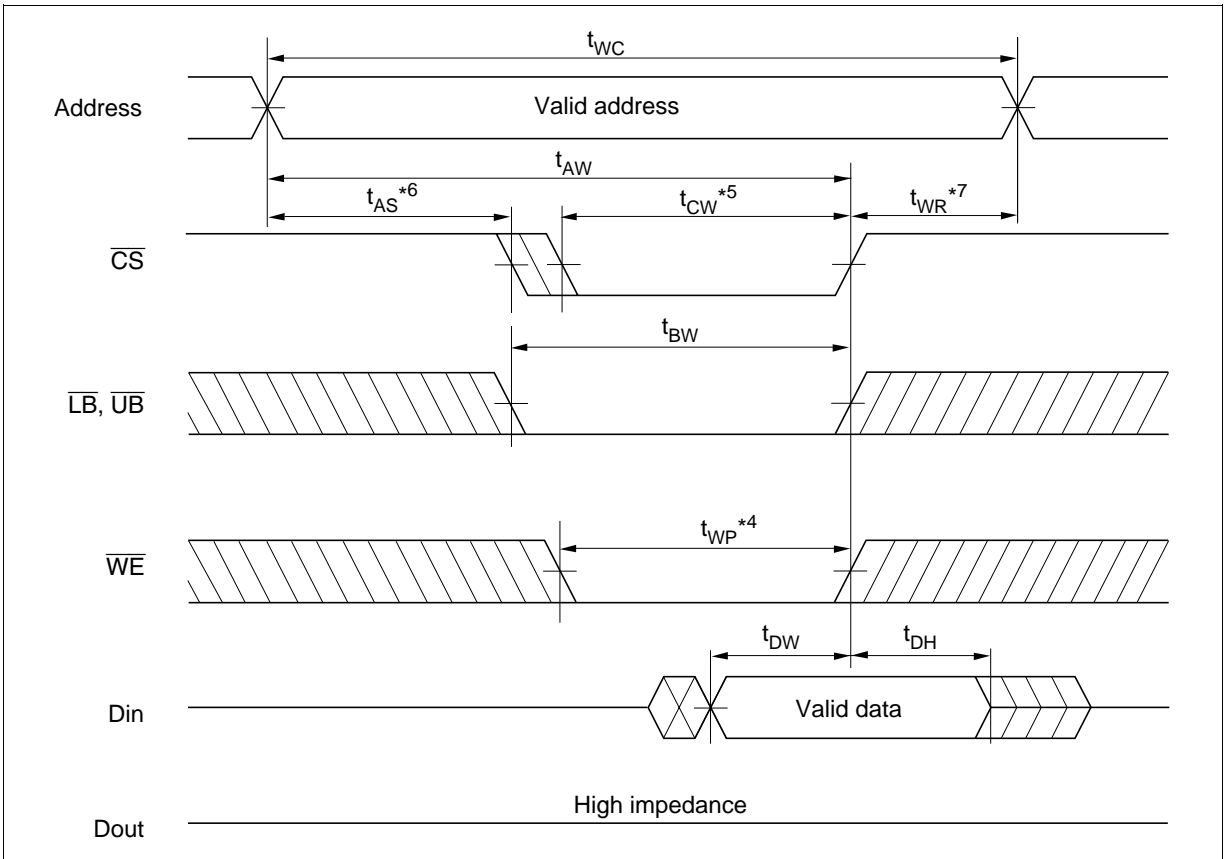
Read Cycle



Write Cycle (1) (\overline{WE} Clock)

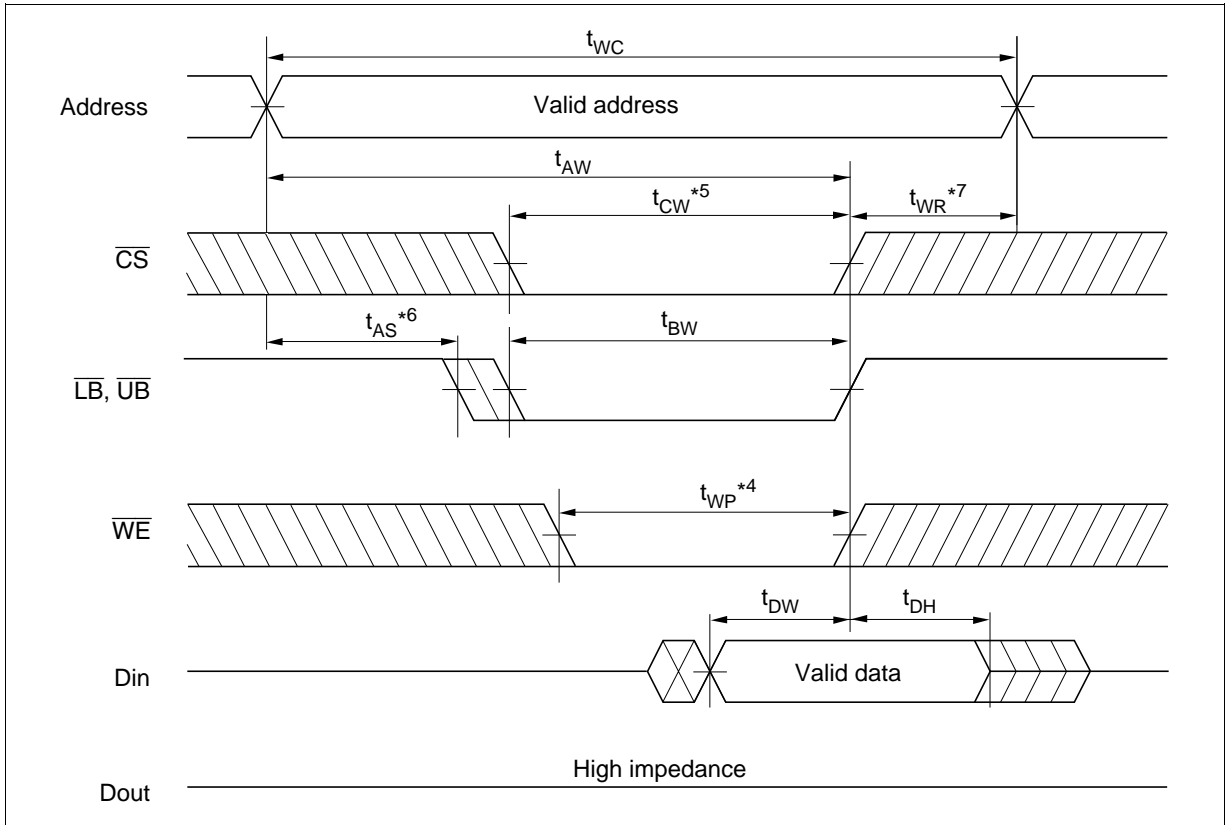


Write Cycle (2) (\overline{CS} Clock, $\overline{OE} = V_{IH}$)



HM62W16258B Series

Write Cycle (3) (\overline{LB} , \overline{UB} Clock, $\overline{OE} = V_{IH}$)

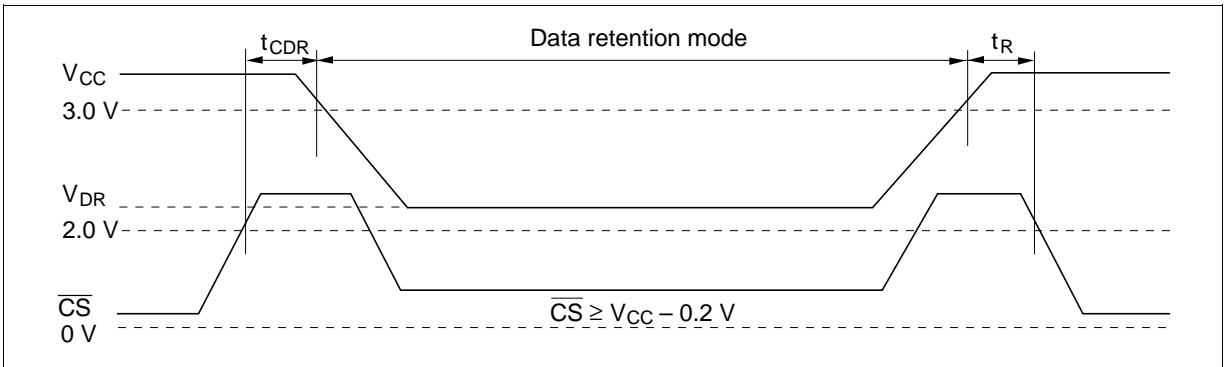


Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

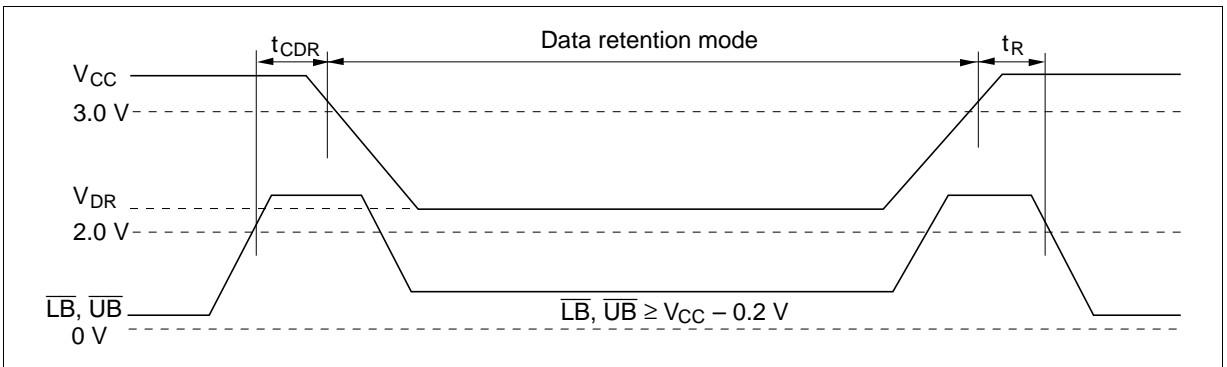
| Parameter | Symbol | Min | Typ ^{*4} | Max | Unit | Test conditions ^{*3} |
|--------------------------------------|-----------------|---------------|-------------------|-----|---------|---|
| V_{CC} for data retention | V_{DR} | 2.0 | — | — | V | $V_{in} \geq 0V$ (1) $\overline{CS} \geq V_{CC} - 0.2 V$ or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 V$ $\overline{CS} \leq 0.2 V$ |
| Data retention current | I_{CCDR}^{*1} | — | 0.8 | 20 | μA | $V_{CC} = 3.0 V, V_{in} \geq 0V$ (1) $\overline{CS} \geq V_{CC} - 0.2 V$ or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 V$ $\overline{CS} \leq 0.2 V$ |
| | I_{CCDR}^{*2} | — | 0.8 | 10 | μA | |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveform |
| Operation recovery time | t_R | t_{RC}^{*5} | — | — | ns | |

- Notes:
1. This characteristic is guaranteed only for L-version, 10 μA max. at $T_a = 0$ to $+40^\circ\text{C}$.
 2. This characteristic is guaranteed only for L-SL version, 5 μA max. at $T_a = 0$ to $+40^\circ\text{C}$.
 3. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, \overline{LB} , \overline{UB} buffer and Din buffer. If \overline{CS} controls data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , \overline{LB} , \overline{UB} , I/O) can be in the high impedance state. If \overline{LB} , \overline{UB} controls data retention mode, \overline{LB} , \overline{UB} must be $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 V$, \overline{CS} must be $\overline{CS} \leq 0.2 V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0 V$, $T_a = +25^\circ\text{C}$ and not guaranteed.
 5. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) (\overline{CS} Controlled)



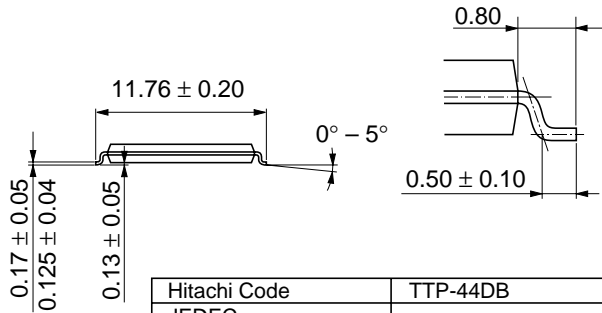
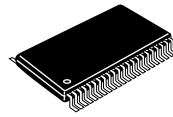
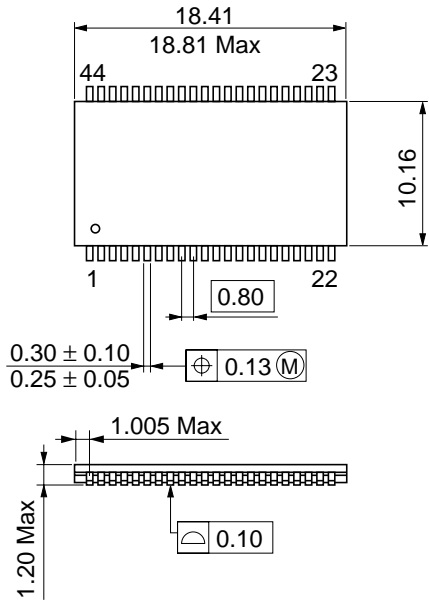
Low V_{CC} Data Retention Timing Waveform (2) (\overline{LB} , \overline{UB} Controlled)



Package Dimensions

HM62W16258BLTT Series (TTP-44DB)

Unit: mm



Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | TTP-44DB |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.43 g |

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